16-bit MEMS Latching Type Photonic Time Delay



(patent pending)







The MEMS Series N-bit (up to 16-bit) Photonic Time Delay digitally varies the delay time inside a fiber with exceptionally large range (maximum delay) and precision (bit). It selectively routes optical signals through N fiber loops whose lengths increase successively by a power of 2. Since each switching element allows the signal to either pass or bypass a fiber loop, a delay T may be inserted, which can take any value (in increments of ΔT) up to the maximum value T.

This is achieved using a patent pending MEMS configuration and activated via an electrical control signal. Latching operation preserves the selected optical path after the drive signal has been removed. The unit is a completed module with built-in driver.

Features

- Up to 18-bit Resolution
- High Reliability
- Direct voltage driving
- Low Insertion Loss
- Low Power Consumption

Applications

- Phase-Array Antennas
- Instrumentation

Specifications

Parameter	Min	Typical	Max	Unit	
Wavelength Band	780	1550	2000	nm	
Fiber Segment Number (bit #)			18	Loop	
Insertion Loss [1]		3	4.5	dB	
Polarization Dependent Loss (SM)		0.1	0.2	dB	
Polarization Extinction Ratio (PM)	18	24		dB	
Cross Talk	40	50		dB	
Return Loss	50	55		dB	
Switching Time (fall, rise)		10		ms	
Delay Time Range	0		m	S	
Polarization Mode Dispersion		0.1	0.2	ps	
Device Type	Latching				
VOA Resolution	Continuous				
VOA PDL		0.15	0.5	dB	
Operating Temperature	-5		70	°C	
Storage Temperature	-40		85	°C	
Optical Power Handling	300				

Notes:

[1]. Input to output with a single delay (1m fiber) loop.

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P +1 781-935-1200

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sales@photonwares.com

www.agiltron.com

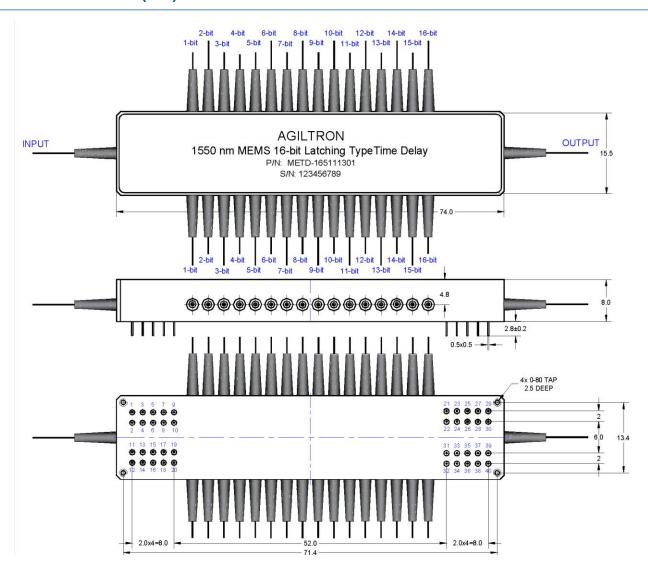
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Mechanical Dimensions (mm)



^{*} Product dimensions may change without notice. This is sometimes required for non-standard specifications.

Electrical Driving Requirements

[1]. 5VDC: 5.0 ± 02 V. Static 3 mA; During Pulse Current is 100 mA. The switch will remain in its previous light path state, if this voltage is removed (latching).

[2]. 5V Pulse: 5.0 ± 02 V. Pulse width is 40 ± 5 ms.

16-bit MEMS Latching Type Time Delay Driving Table

TBD



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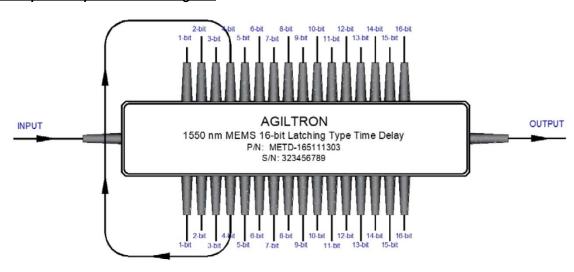


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Electrical Driving Requirements

5-bit Optical loop Connection Diagram:



Ordering Information

				1			0	
Prefix	Туре	Wavelength	Configuration	Switch type	Fiber Type	Fiber Cover	Delay Range	Connector
METD- ^[1]	11-Bit = 11 12-Bit = 12 13-Bit = 13 14-Bit = 14 15-Bit = 15 16-Bit = 16 Special = 00	1260~1620 = B 1310nm = 3 1510nm = 5 Special = 0	Standard = 1 Special = 0	Latching = 1 Special = 0	SMF-28 = 1 PM1550 = B PM1310 = D PM980 = E PM850 = F Special = 0	Bare fiber = 1 0.9mm tube = 3 Special = 0	Customized = 0	None = 1 FC/PC = 2 FC/APC = 3 SC/PC = 4 SC/APC = 5 ST/PC = 6 LC/PC = 7 Duplex LC/PC = 8 LC/UPC = U Special = 0

[1]. METD: MEMS Variable Time Delay.

Fiber Core Alignment

Note that the minimum attenuation for these devices depends on excellent core-to-core alignment when the connectors are mated. This is crucial for shorter wavelengths with smaller fiber core diameters that can increase the loss of many decibels above the specification if they are not perfectly aligned. Different vendors' connectors may not mate well with each other, especially for angled APC.

Fiber Cleanliness

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Fibers with smaller core diameters (<5 µm) must be kept extremely clean, contamination at fiber-fiber interfaces, combined with the high optical power density, can lead to significant optical damage. This type of damage usually requires re-polishing or replacement of the connector.

Maximum Optical Input Power

Due to their small fiber core diameters for short wavelength and high photon energies, the damage thresholds for device is substantially reduced than the common 1550nm fiber. To avoid damage to the exposed fiber end faces and internal components, the optical input power should never exceed 20 mW for wavelengths shorter 650nm. We produce a special version to increase the how handling by expanding the core side at the fiber ends.